REMARKS

The indication of allowable subject matter in claim 3 is acknowledged and appreciated. In view of the following remarks, it is respectfully submitted that all claims are in condition for allowance.

Claims 1 and 2 stand rejected under 35 U.S.C. § 102 as being anticipated by Asami '100, and claims 4-8 stand rejected under 35 U.S.C. § 103. Claim 1 is independent. These rejections are respectfully traversed for the following reasons.

Claim 1 recites in pertinent part, "direct memory access circuit ... ." The Examiner alleges that UART 6 of Asami "acts as the DMA circuit (col. 3, lines 27-36, col. 4, lines 27-45)." However, it is respectfully submitted that it is well known in the art that a UART is NOT equivalent to a DMA circuit. That it, a direct memory access circuit is readily recognized as a circuit which can implement a "method of transferring data from one memory area to another without having to go through the central processing unit" (*see* copy of techdictionary.com attached hereto). Whereas, a UART merely operates to convert a serial data signal to a parallel data signal. A UART does not have the capability to transfer data from one memory to another without a CPU. In fact, as expressly disclosed at col. 4, lines 35-37 of Asami, the UART 6 supplies the converted signal to a ***control circuit unit*** 8 which controls the memory unit operation. Accordingly, UART 6 does not function as a DMA circuit.

In order to expedite prosecution, Applicants' representative initiated a telephone interview with Examiner Koyama to discuss this matter. Applicants and Applicants' representative would like to thank Examiner Koyama for her courtesy in conducting the interview and for her assistance in resolving issues. During the interview, Applicants emphasized that an ordinary artisan would readily recognize that a UART is not equivalent to a DMA circuit. In response, the Examiner referenced prior art that she alleged showed a UART

which can operate as a DMA. These references have been listed on the Interview Summary Record dated October 14, 2003 (i.e., USP No.'s: 6434161 to Higbee et al., 6615167 to Devins et al., 6625683 to Khan et al., and 6563618 to Morrow et al.). **It is respectfully submitted that in response to this amendment, the Examiner list the prior art she has referenced in the Interview Summary dated October 14, 2003 on a PTO-892 form to make them formally of record in this application.**

It is respectfully submitted that none of these references suggest that DMA circuits and UART's are equivalent. Instead, it is respectfully submitted that these references further support that a UART and DMA are distinct electrical circuits. The cited references merely disclose, at best, that a UART can be ***supplemented*** to work together with a DMA circuit so as to perform a dual function. For example, turning to col. 1, lines 39-41 of USP No. 6,434,161 to Higbee et al., the definition of a conventional UART is given as a "device [which] essentially converts data between parallel and serial formats .... ." Higbee et al. goes on to state at col. 5, lines 27-31 that the disclosed UART is an "***[e]mulated*** UART [that] is not implemented as a traditional hardware FIFO ... as [in a conventional UART] described in Figure 1, but rather is implemented ... as a ***combination*** of hardware and firmware which implements a Direct Memory Access-like (DMA) transfer ..." (emphasis added). That is, a UART can be supplemented with hardware to provide DMA functionality, but a conventional UART as disclosed in Asami does not have a DMA function. The remaining prior art references at most further emphasize the aforementioned point. For example, col. 3, lines 38-41 of USP No. 6,615,167 to Devins et al. corresponding to Figure 1 thereof further evidences that DMA circuits and UART circuits are recognized in the art as being capable of operating together in a common design yet are individually ***distinct*** entities.

Turning to Asami, the disclosed UART 6 merely functions to convert the data signal specifically for supplying the data to the controller 8. Accordingly, the UART 6 of Asami expressly does not have DMA functionality. Moreover, the controller 8 is an integral and essential element of the disclosed IC card for controlling the buffer (*see, e.g.*, Abstract of Asami). Accordingly, Asami teaches away from accessing the memory without a controller, let alone suggest adding the necessary hardware to implement DMA functionality in the UART 6.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Asami does not anticipate claim 1, nor any claims dependent thereon.

The rejections under 35 U.S.C. § 103 rely on the same interpretation of Asami and are therefore improper for at least the same reasons discussed above. The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in the pending claims because the proposed combinations fail the "all the claim limitations" standard required under § 103. Based on all the foregoing, it is submitted that claims 1-8 are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 102 and 103 be withdrawn.

CONCLUSION

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Ramyar M. Farid
Registration No. 46,692

OFFICIAL

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 RMF:MWE
Facsimile: (202) 756-8087
Date: December 8, 2003

Certification of Facsimile Transmission
I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.
Ramyar Farid
Type or print name of person signing certification
12/8/03
Signature Date

techdictionary.com

Home
Search
Search Tips
Domain List
Chat/SMS Terms
Emoticons
File Extensions
Suggest Term
Bookmark Us
Add To Your Site
TechTips & Links
Tech News
Virus News
Advertise
About/Site Map

Search Results

Term:	Definition:
Direct Memory Access/Addressing	(DMA). A method of transferring data from one memory area to another without having to go through the central processing unit.

SEARCH -AGAIN